Pipeline stages registers:

IF/ID: 66 bit

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| NXT PC (32bit) | Unpredicted PC(32bit) | Inst.(32 bit) | INT(1 bit) | RST(1 bit) |

ID/EX:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NXT PC (32bit) | Src1 code(3bits) | src1 data (32bit) | Src2 code(3bits) | src2 data (32bit) | Dst code(3bit) | Immediate field (32 bit) | EA (20 bit) | TMP (32bit) | Unpredicted PC(32bit) | INT(1 bit) | RST(1 bit) | RST(1 bit) |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NXT PC (32bit) | I/O in(32bit) | Flags(4bits) | Op code (5 bits) | ALU result (32 bit) | DST CODE  (3 bit) | Src1 code(3bits) | Src2 code(3bits) | Unpredicted PC(32bit) | INT(1 bit) | RST(1 bit) |

EX/MEM:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Op code(5 bits) | ALU RESULT  (32 bit) | Rs(mem read) (32 bit) | DST CODE  (3 bit) | INT(1 bit) |

MEM/WB: